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Development of X-ray Metrology for Advanced CFET Logic and 3D-DRAM Devices

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The semiconductor industry's drive for better power, performance, area, and cost (PPAC), accelerated by AI's insatiable demand for computing and memory is increasingly enabled by 3D device architectures and vertical scaling. In logic, gate-all-around (GAA) is progressing toward complementary FET (CFET) transistors, which vertically stack n- and p-type devices using Si/SiGe multilayers. In memory, emerging 3D-DRAM pushes these multilayers even further, potentially requiring hundreds of Si/SiGe pairs. Both technologies depend on engineered substrates with epitaxial Si/SiGe multilayers on Si wafers, making this a critical and challenging starting point of the fabrication process flow. Layer parameters such as Ge content, thickness, and interface width define the process window for downstream steps such as selective etching.

Defects in blanket wafers can ultimately cause device failure and must be identified before patterning to avoid losing weeks of product. Thick 3D-DRAM stacks are especially prone to strain relaxation, generating dislocations or lattice undulations that propagate through the multilayer and degrade performance or yield. X-ray diffraction imaging (XRDI) provides rapid, non-destructive visualization of crystalline defects and is highly sensitive to early-stage relaxation. Such relaxation can generate linear defects that originate at wafer edges and move inward as Si/SiGe pair count increases. Fully automated XRDI covering wafer handling, measurement, and analysis enables high-throughput characterization of tens of wafers per hour with no operator intervention after setup. We will discuss common semiconductor killer defects and how XRDI enables in-line defect detection at production-level throughputs.

For detailed layer-by-layer characterization, fitting of HRXRD and XRR data yields Ge composition, layer thickness, and inter-layer roughness. Accuracy improves further when HRXRD and XRR are combined in a hybrid analysis, where XRR constrains thickness and HRXRD determines composition, reducing parameter correlations and accelerating fitting, enabling more precise metrology for in-line process control. Reciprocal space maps (RSMs) with modern 2D detectors can measure additional valuable information for characterizing process issues during development and ramp of epitaxial deposition processes. We will show how advances in HRXRD / XRR hybrid analysis and RSM-based characterization support the development and manufacturing of increasingly complex 3D device structures and help leading edge logic and memory suppliers to meet rising production demands in the AI era.